spectracom

TSync Series

TIME CODE PROCESSOR
with optional GNSS RECEIVER

User Manual

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Five Year Limited Warranty

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This warranty shall not apply if the product is used contrary to the instructions in its manual or is otherwise subjected to misuse, abnormal operations, accident, lightning or transient surge, or repairs or modifications not performed by Spectracom authorized personnel.

Items with a variance to the Five Year Warranty Period are as follows:

90 Days Warranty

TimeKeeper Software
VelaSync Hardware

One Year Limited Warranty

Timeview Analog Clock
Path Align-R Products
Bus-level Timing Boards
IRIG-B Distribution Amplifiers
Down-Up Antenna Converter (DUC)
Geo-iNav/Geo-PNT

Two Year Limited Warranty

Rubidium Oscillators
Epsilon Board EBO3
Epsilon Clock 1S, 2S/2T, 3S, 31M
Epsilon SSU
Power Adaptors
Digital and IP/POE Clocks
WiSync Wireless Clock Systems and IPSync IP Clocks
Rapco 1804, 2804, 186x, 187x, 188x, 189x, 2016, 900 series

Three Year Limited Warranty

Pendulum Test & Measurement Products GPS-12R, CNT-9x, 6688/6689, GPS-88/89, DA-35/36, GPS/GNSS Simulators

Country Variances

All Spectracom products sold in India have a one year warranty.

Warranty Exclusions

Batteries, fuses, or other material contained in a product normally consumed in operation.

Shipping and handling, labor & service fees

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Extended Warranty Coverage

Extended warranties can be purchased for additional periods beyond the standard warranty. Contact Spectracom no later than the last year of the standard warranty for extended coverage.

Warranty Claims

Spectracom's obligation under this warranty is limited to the cost of in-factory repair or replacement, at Spectracom's option, of the defective product or the product's defective component. Spectracom's Warranty does not cover any costs for installation, reinstallation, removal or shipping and handling costs of any warranted product. If in Spectracom's sole judgment, the defect is not covered by the Spectracom Limited Warranty, unless notified to the contrary in advance by customer, Spectracom will make the repairs or replace components and charge its then current price, which the customer agrees to pay.

In all cases, the customer is responsible for all shipping and handling expenses in returning product to Spectracom for repair or evaluation. Spectracom will pay for standard return shipment via common carrier. Expediting or special delivery fees will be the responsibility of the customer.

Warranty Procedure

Spectracom highly recommends that prior to returning equipment for service work, our technical support department be contacted to provide troubleshooting assistance while the equipment is still installed. If equipment is returned without first contacting the support department and "no problems are found" during the repair work, an evaluation fee may be charged.

Spectracom shall not have any warranty obligations if the procedure for warranty claims is not followed. Customer must notify Spectracom of a claim, with complete information regarding the claimed defect. A Return Authorization (RMA) Number issued by Spectracom is required for all returns.

Returned products must be returned with a description of the claimed defect, the RMA number, and the name and contact information of the individual to be contacted if additional information is required by Spectracom. Products being returned on an RMA must be properly packaged with transportation charges prepaid.

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CHAPTER 1

Product Overview

Figure 1-1: TSync Series Time Code Processors

The following topics are included in this Chapter:

1.1 Introduction

Spectracom TSync Time Code Processors with optional internal GNSS receiver are complete bus-level synchronized time code processing boards that support multiple timing, frequency and event inputs and outputs. Inputs used as a timing reference can be configured such that the TSync Time Code Processor automatically switches to the next lower-priority input when the current timing reference is lost, thus providing uninterrupted service.

The onboard oscillator is capable of providing a 5ns resolution, and is typically disciplined by and phase-locked to an external timing input

In the absence of any valid external timing references this 10 MHz oscillator, central to the TSync Time Code Processor timing functions, provides holdover functionality, thus allowing the TSync Time Code Processor to continue serving time and frequency, until an external reference becomes available again.

The TSync Time Code Processor generates an IRIG AM and IRIG DCLS output pair, as well as 10 MHz sine wave and 1PPS outputs.

The four programmable inputs may be used as event capture inputs, dedicated to your time-tagging applications. Four user-programmable alarm and frequency outputs are provided as well. Programmable output functions include a periodic pulse or “heartbeat,” square wave, and a programmable start/stop time “alarm” output.

Key to the TSync Time Code Processor's functionality is the ability to generate interrupts. Using one of the many available Spectracom driver packages, you may configure your card using interrupt-driven algorithms to support your custom application.

1.2 General Specifications

Table 1-1: TSync family: system specifications and options (x = YES; o = NO)

	PCIe	cPCI	VPX	PMC	PCI-104
Form factor	Low-profile PCIe; full-height mounting bracket provided	Compact PCI (cPCI) Compliant to PICMG 2.0 r3.0 100 mm x 160 mm (3U card size)	3U VPX form factor Compliant to VITA-46 100 mm x 160 mm	Single-size CMC (Common Mezzanine Card) 149 mm x 74 mm	Compliant to PCI-104 spec. r 1.1 Compliant to PCI spec. r 2.2
Bus interface	PCIe x1	Universal Signaling Voltage 3.3 V/5 V	PCIe x1, R1.1 Connectors to VITA 46.0 for P0, P1, and P2	Universal Signaling Voltage 3.3 V/5 V	Universal Signaling Voltage 3.3 V/5 V

	PCIe	cPCI	VPX	PMC	PCI-104
Bus speed	Single-Lane (x1) PCIe; compliant with PCIe Base Spec. R1.1	32-bit address @ 33/66 MHz	Single-Lane (x1) PCIe; compliant with PCIe Base Spec. R1.1	32-bit address @ 33/66 MHz	32-bit address @ 33/66 MHz
GNSS timing module	72-channel receiver with concurrent constellation reception				
Conduction Cooling	O	ANSI/VITA 30.1-2002	VITA 46/IEEE 1101.2	ANSI/VITA 20-2001	O
Thermal frame *(optional)*	O	Standard thermal frames available. Component elevations for custom frame design available upon request.		O	O
Onboard temp. sensor	O	X	X	X	X
Conformal coating *(optional)*	X	X	X	X	X
Custom backpanel I/O	O	X	X	X	O
Weight	122 g	173 g (w/o thermal frame) 323 g (w/ thermal frame)	179 g (w/o thermal frame) 329 g (w/ thermal frame)	88 g	96 g
Oscillators:					
TCXO	X	X	X	X	X
OCXO	X	X	X	X	X
Rugged OCXO	O	X	X	O	O
References:					
IRIG/Other	X	X	X	X	X
Internal GNSS	X	X	X	X	X
External GNSS	X	X	O	O	O
Internal SAASM GPS	O	X	X	O	O

1.3 Power Consumption

Table 1-2: Board power consumptions (**typical**)

@ V_{DC}	PCIe	cPCI	VPX	PMC	PCI-104
+3.3 V (±5%)	0.7 A	0.7 A	Vs2: 0.85 A (+5%/-2%)	0.7 A	0.7 A
+5V (±5%)	n/a	1.4 A	Vs3: (+5%/-2.5%) TCXO, OCXO options: 0.4 A Rugged OCXO option: 0.6 A [Rugged OCXO: max. (warm-up): 1.4 A]	1.4 A	1.4 A
+12 V (±8%)	0.2 A	0.2 A	Vs1: 0.2 A (±5%)	0.2 A	0.2 A
–12 V (±5%)	n/a	0.2 A	12V_AUX: -0.2 A	0.2 A	0.2 A

1.4 Temperature Sensor

With the exception of the PCIe model, all TSync boards are equipped with an on-board temperature sensor:

- **Operating temperature range**: -40°C to 85°C (-40°F to 185°F)
- **Accuracy**: ±3°C max.
- **Update rate**: Once per second.

1.5 Input/Output Specifications

1.5.1 Inputs

1.5.1.1 1PPS Input

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **1Hz pulse**, rising edge or falling edge active (selectable)
  - 100 ns minimum **pulse width**
- **Amplitude**: 0 V to +5.5 V input range, +0.8 V_{VIL}, +2.0 V_{VIH}
- **Input impedance** <150 pF capacitive

1.5.1.2 IRIG AM Input

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- Accepts IRIG **formats** A, B, G; NASA36; IEEE 1344
- **Amplitude**: 500 mV_{p-p} to 10 V_{p-p}
- **Modulation ratio**: 2:1 minimum, 6:1 maximum
- **Input impedance**: 10 kΩ minimum
- DC **Common Mode Voltage**: ±150 V_{DC} maximum
- **Input Stability**: Better than 100 ppm

1.5.1.3 IRIG DCLS Input

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- Accepts IRIG **formats** A, B, G; NASA36; IEEE 1344 pulse width codes (does not accept Manchester modulated codes)
- RS-485 **differential input**: –7V to +12 V common mode voltage input range, 200 mV_{p-p} differential voltage threshold
- **Single-ended input**:
  - +1.3 $V_{VIL\ min}$, +2 $V_{VIH\ max}$
  - +1.45 $V_{VIL\ typ}$, +1.85 $V_{VIH\ typ}$

1.5.1.4 GPIO Inputs

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **Amplitude**: 0V to +5.5 V input range, +0.8 V_{VIL}, +2.0 V_{VIH}
- **Polarity** (selectable): Positive or negative

- **Input impedance**: <150 pF capacitive
- 50 ns active **pulse width** minimum; 50 ns minimum between pulses
- **Repetition rate**. More than 10,000 events per second
- **Resolution**: 5 ns

1.5.2 Outputs

1.5.2.1 1PPS Output

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **1Hz pulse**, rising edge or falling edge active (selectable)
  - 40 ns to 900 ms active **pulse width** (selectable, 200 ms default)
- **Rise time**: <10 ns
- **Signal level**: TTL compatible, 4.3 V_{min}, base-to-peak into 50 Ω
  [PCIe only: TTL compatible, 2.2 V minimum, base-to-peak into high impedance]
- **Accuracy**: Positive edge within ±[X] nanoseconds of UTC when locked to a valid 1PPS input reference (for [X], see table below).

Table 1-3: 1PPS output accuracy

	TCXO	OCXO	OCXO (Rugged Option, cPCI & VPX only)
Accuracy to UTC (1-sigma locked to GPS)	±50 ns	±50 ns	±25 ns
Holdover (constant temp after 2 weeks of GNSS lock)			
After 4 hours	12 µs	3 µs	1 µs
After 24 hours	450 µs	100 µs	25 µs

1.5.2.2 10 MHz Output

10 MHz sine wave output from oscillator

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **Output impedance**: 50 Ω nominal
- **Output load**: 50 Ω minimum
- **Output harmonics**: < -40 dBc
- **Output spurious**: < -70 dBc

10 MHz LVDS Clocks via P2 Connector (VPX only)

- Four (4) LVDS differential pairs
- **Impedance**: 100 Ω
- **Duty cycle**: 50%
- **Rise time**: <10 ns

Table 1-4: 10 MHz output specifications

	TCXO	OCXO	OCXO (Rugged Option, cPCI & VPX only)
Accuracy (average over 24 hours when GNSS locked)	$1x10^{-11}$	$5x10^{-12}$	$2x10^{-12}$
Medium term stability (without CPS after 2 weeks of GNSS lock)	$1x10^{-8}$/ day	$2x10^{-9}$/ day	$5x10^{-10}$/ day
Phase noise (dBc/Hz)			
@1 Hz	—	–85	—
@10 Hz	—	–113	–120
@100 Hz	–110	–120	–135
@1 KHz	–135	–140	–135
@10 KHz	–140	–150	–145
Signal wave form & levels	+13 dBm ±3dB into 50 Ω, BNC		

1.5.2.3 IRIG AM Output

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **Output formats** A, B, E (100 Hz, 1 kHz), G; NASA36; IEEE 1344
- **Amplitude**:
  - 0.5 V_{p-p} to 6 V_{p-p} into 50 Ω, user settable
  - 1V_{p-p} to 12 V_{p-p} into > 600 Ω
- **Output impedance**: 50 Ω nominal
- **Output load**: 50 Ω minimum
- **Modulation ratio**: 3:1 nominal
- **Accuracy**: ±2 to 200 microseconds (IRIG-format dependent)

1.5.2.4 IRIG DCLS Output

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

- **Outputs formats**: A, B, E, G; NASA36; IEEE 1344 pulse width codes (does not generate Manchester modulated codes)
- RS-485 **differential signal**:
  - 1.8 V_{max} common mode output voltage (RS-485 compatible)
  - 1.5 V_{min} to 3.3 V max differential output voltage swing
- Single-ended **amplitude** (100 Ω load):
  - 0.5 V_{VOL} max, +2.5 V_{VOH} min (TTL compatible)

1.5.2.5 GPIO Outputs

Available through the **timing connector**, see "Connectors & Pinouts" on page 16 for details.

Periodic Output:

- **Amplitude**: TTL compatible, 4.3 V_{min}, base-to-peak into 50 Ω
  [PCIe only: 2.2 V minimum, base-top-peak into high impedance]
- **Pulse width**: 50 ns to 999 ms active pulse width, in 20 ns increments
- **Period**: 100 ns min, 60 s max, in 20 ns increments
- **Polarity** (selectable): Positive or negative

Time-Match/Alarm Output

- **Amplitude**: TTL compatible, 4.3 V minimum, base-to-peak into 50 Ω; 2.2 V minimum, base-to-peak into high-impedance
- **Range**: 100 days in 5 ns steps

1.6 GNSS Receiver Specifications

TSync Time Code Processors are capable of utilizing GPS/GNSS timing signals as an external reference. To this end, all models can be ordered with either an optional **internal** GNSS receiver, or the TSync PCIe and cPCI models can be configured—at the time of purchase—for use with an **external** GNSS receiver (integrated into the antenna housing).

1.6.1 Internal GNSS Receiver

All TSync Time Code Processor models are available with an optional onboard GNSS receiver (to be ordered at the time of purchase; factory retrofits may be possible.)

If installed, the board supplies $5V_{DC}$ through the GNSS receiver to the external antenna via the coaxial cable (antenna and cable are sold separately).

Alternatively, TSync PCIe and cPCI boards can also be operated with an **external** GNSS receiver (i.e., the receiver is built into the antenna housing). In this case, the board supplies 12 V_{DC} to the receiver/antenna through its data communications cable.

- **Receiver type**:
  - 72-channel receiver with concurrent dual-constellation reception; pre-configured to receive GPS/QZSS & GLONASS
  - Supports GPS/QZSS L1 C/A, GLONASS L1, BeiDou B1 Galileo-ready E1 (subject to firmware upgrade)
- **Acquisition times**:
  - Cold start – GPS & GLONASS: 26 s; GPS & BeiDou: 27 s
  - Aided cold start – GPS & GLONASS: 2 s; GPS & BeiDou: 3 s
- **Sensitivity**:
  - Tracking & Nav – GPS & GLONASS: -167 dBm; GPS & BeiDou: -165 dBm
  - Reacquisition – GPS & GLONASS, GPS & BeiDou: -160 dBm
- **Timing accuracy**, clear sky: ≤ 20 ns
- **Time-pulse frequency**: 0.25 Hz – 10 MHz
- **Time-pulse jitter**: ±11 ns
- **Time-mark resolution**: 21 ns
- **Integrity reports**: RAIM active, phase uncertainty time-pulse rate/duty-cycle.

Antenna Connection

All TSync Time Code Processor equipped with the optional on-board GNSS receiver have a front panel SMA **RF connector**, through which the signal from, and the supply power to the GNSS antenna (sold separately) are provided (supply power: +5V [±10%] @ 30 mA max).

The RF antenna cable (sold separately) is connected to the TSync Time Code Processor board via a short male-SMA-to-Type-N adapter cable (included), made from RG-316 coaxial cable.

Note: The provided cable should be used instead of 3rd party adapter, as it incorporates a strain relief, protecting the connectors.

1.6.2 External GNSS Receiver

PCIe and **cPCI** boards can be operated with an external GNSS receiver, i.e. the receiver is integrated into the **Acutime GG** smart antenna unit.

A high-density DB-15 connector is used to connect the external antenna (with its built-in GNSS receiver) to the board. With external receivers, cable lengths up to 90 m (300 ft.) are possible.

Electrical Characteristics, Board to Receiver Transmission

RS-485 Differential Signal:

- +1.5 V to +2V Common Mode Output Voltage
- 1.5 V min to 3.3 V max Differential Output Voltage Swing

Electrical Characteristics, Receiver to Board Transmission

RS-485 Differential Input:

- -7 V to +12 V common mode voltage input range, 200 mV_{p-p} differential voltage threshold

Electrical Characteristics, Receiver Power

- 50 mA @ 12 V provided to power the antenna

Specifications, external GNSS receiver

- **Acquisition time**:
  - < 4 minutes from a cold start
  - Re-acquisition time: < 2 sec (90%; current almanac downloaded)
- **Frequency**:
  - GPS L1 (1575.42 MHz)
  - GLONASS L1 (1602 MHz)
- **Satellites tracked**: up to 32 simultaneously
- **Sync to UTC**: within ±15 ns to GPS/UTC (1 sigma) (stationary)
- **Sensitivity**: -136 dBm (acquisition), -141 dBm (tracking)
- **1PPS accuracy** (1-sigma): <15 ns (stationary mode), <45 ns (mobile operation)
- **Accuracy horizontal position**: <6 meters (50%) <9 meters (90%)
- **Accuracy altitude position**: <11 meters (50%) <18 meters (90%)

1.6.3 SAASM Receiver

cPCI and VPX boards are compatible with a SAASM receiver for authorized users. Instructions specific to SAASM operation are provided in a separate manual. The SAASM receiver is not compatible with GLONASS.

Receiver type: MPE-S Type II GB-GRAM

Frequency: L1 (1575.42 MHz) and L2 (1227.6 MHz) simultaneous; L1- C/A, P(Y); L2 - P(Y)

Satellite Tracking: 1 to 12

TTFF – Time to First Fix (Synchronization Time):

- Cold Start (with almanac download): 15 minutes
- Cold Start (no almanac download): 5 minutes
- Warm Start: 90 seconds
- Hot Start: 10 seconds

TTSF – Time to Subsequent Fix (Reacquisition Time):

- < 20 seconds, Off or Stby < 15 minutes
- < 25 seconds, Off or Stby < 60 minutes
- < 70 seconds, Off < 60 minutes

Antenna connector:

- Convection Cooled: SMA Jack (+3.3 V @ 9 mA to 60 mA)
- Conduction Cooled: SMB Jack (+3.3 V @ 9 mA to 60 mA)

1PPS accuracy: ±100 ns

Key fill: DS102 standard, DS101 optional

Backup Battery: SAASM I/O connector or P1-VBAT, VPX P1 connector.

1.7 PCI-104 Board Dimensions

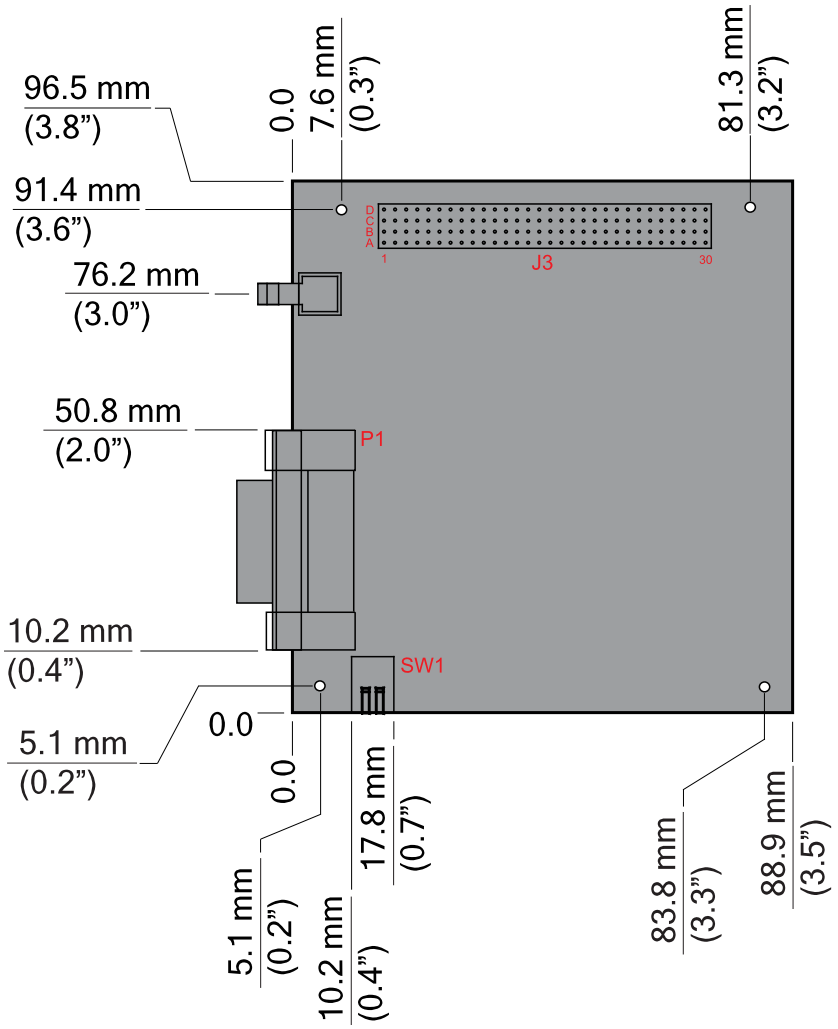

Figure 1-2: Board layout and dimensions

1.8 Environmental Specifications

- **Temperature**:
  - With convection cooling: Operating: –40°C to 75°C (–40°F to 167°F)
  - With conduction cooling: Operating: –40°C to 80°C (–40°F to 176°F)
  - Storage: –40°C to 85°C (—0°F to 185°F)
- **Humidity**, operating and storage:
  - 10% to 95% relative humidity, non-condensing @ 40°C
- **Altitude**:
  - Operating: Up to 10,000 feet
  - Storage: Commercial shipping altitudes supported

1.9 Compliance

This equipment has been tested and found to comply with the following standards:

EMC:

CISPR 11 (2003): Radiated and Conducted Emissions

EN-61236-1: 2006 Consisting of:

- EN61000-3-2 (2000): Harmonic Current Emissions
- EN61000-3-3 (2002): Voltage Fluctuations and Flicker in Low Voltage
- EN61000-4-2 (2001): Electrostatic Discharge Immunity
- EN61000-4-3 (2002): Radiated Electric Field Immunity
- EN61000-4-4 (2004): Electric Fast Transit Burst Immunity
- EN61000-4-5 (2001): High Voltage Surge Immunity
- EN61000-4-6 (2003): RF Common Mode Immunity
- EN61000-4-11 (2004): Voltage Dip and Interrupt Immunity

Supplementary information

This product complies with the requirements of the **Low Voltage Directive 2006/95/EC** and the **EMC Directive 2004/108/EC**, and with the European Union Directive **2002/95/EC** on the Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS).

Electro-magnetic compliance/FCC

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense.

CHAPTER 2

Connector Pinouts

This topic describes the pinouts of the:

- timing connector
- antenna connector
- backplane connectors (if available).

2.1 Connectors & Pinouts

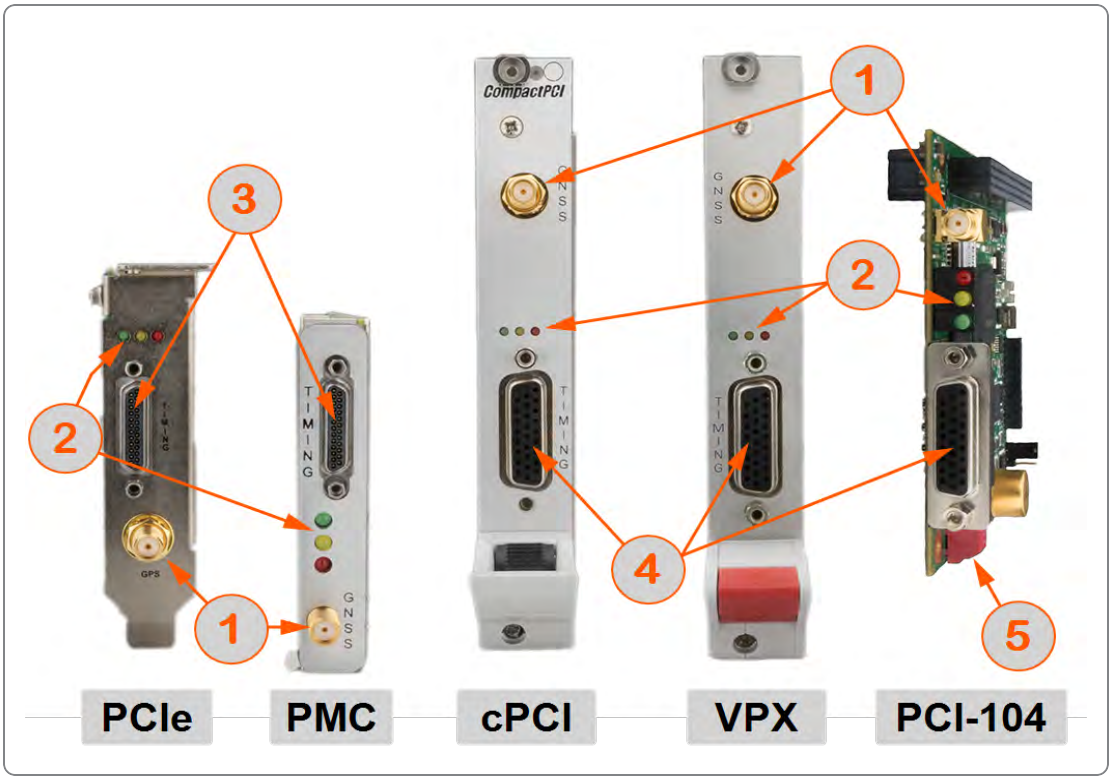

Figure 2-1: TSync faceplates

NOTES:
PCIe shown with half-height faceplate.
All units shown without thermal frames.
All units shown with internal GNSS receivers.

Table 2-1: Legend faceplate illustration

No.	Function	Type	For additional information, see:
1	GNSS antenna connection	SMA RF	n/a
2	Status LEDs	green/yellow/red	"Status LEDs" on page 26
3	Timing connector	25-pin micro D-sub	"Timing Connector Pinouts" on the facing page
4	Timing connector	26-pin high density D-sub	
5	Multi-stack PCI no. configuration	DIP switch SW1	"PCI-104 Configuration (DIP Switch)" on page 26

2.2 Timing Connector Pinouts

The timing interface connector supports all of the input and output references, as well as General-Purpose Input/Output (GPIO) functionality. Depending on your board model, it consists either of a 26-pin High-Density D-Sub connector, or a 25-pin Micro D-Sub connector.

Table 2-2: Timing connector pinout

Pin	Signal	Pin	Signal
1	GPIO Output 2	14	GPIO Output 3
2	Ground	15	Ground
3	GPIO Output 0	16	GPIO Output 1
4	GPIO Input 2	17	GPIO Input 3
5	Ground	18	Ground
6	GPIO Input 0	19	GPIO Input 1
7	External 1PPS Input	20	1PPS Output
8	Ground	21	Ground
9	IRIG AM Output	22	10 MHz Output
10	IRIG AM Input +	23	Ground
11	IRIG AM Input	24	IRIG DCLS Input -
12	IRIG DCLS Output	25	IRIG DCLS Input +
13	IRIG DCLS Output +	(26)	Ground

Note: All units are shipped with a breakout cable; for additional information, see "Accessories & Options" on page 46.

Note: Units with a 25-pin micro D-sub connector are shipped with a strain-reducing adapter cable; for additional information, see "Accessories & Options" on page 46.

2.3 External Antenna Connector: Pinout

PCIe and cPCI boards can be ordered in a configuration that allows operating these boards with an external GNSS receiver. In both cases, an adapter cable is used to connect the serial antenna cable with the corresponding board interface connector:

- cPCI: 15-pin high density D-Sub
- PCIe: Mini-DIN 8

The tables and illustrations below depict the pinouts for either connector.

cPCI Adapter Cable Pinout

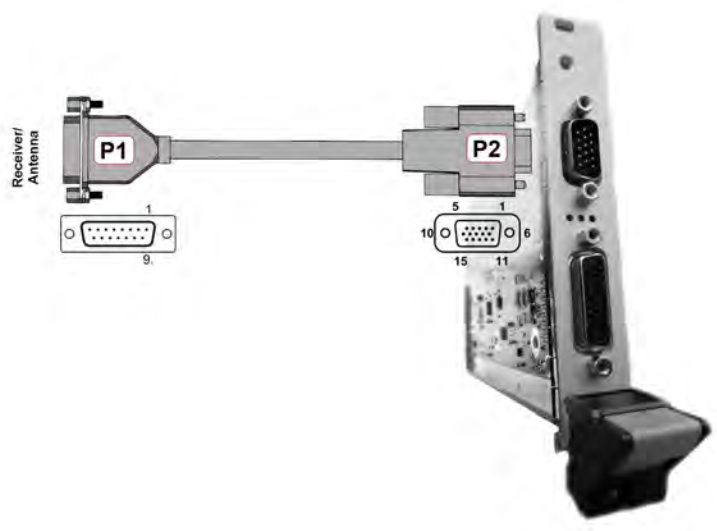

Figure 2-2: cPCI: Adapter cable for external GNSS receiver

	Signal	P1, pin no.	P2, pin no.
PAIRED	+12 V	3	8
	GND	5	7
PAIRED	1PPS +	9	4
	1PPS –	14	5
PAIRED	UP +	12	1
	UP –	13	2
PAIRED	DOWN +	10	11
	DOWN –	11	12
FOIL AND DRAIN WIRE	SHIELD	SHELL	SHELL

PCIe Adapter Cable Pinout

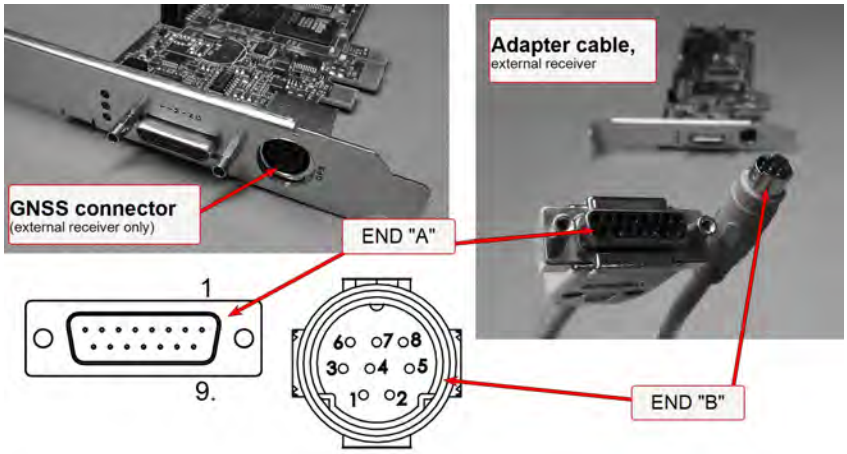

Figure 2-3: PCIe: Adapter cable for external GNSS receiver

Signal	END "A"	END "B"
+12 V	3	1
GND	5	2
1PPS +	9	6
1PPS –	14	3
UP +	12	8
UP –	13	5
DOWN +	10	4
DOWN –	11	7
SHIELD	SHELL	SHELL

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CHAPTER 3

Installation

Caution: Read the Safety Instructions before beginning with the installation: See "YOUR SAFETY" on page ii.

The following topics are included in this Chapter:

3.1 ESD: Best Practices

Caution: Electronic equipment is sensitive to Electrostatic Discharge (ESD). Observe all ESD precautions and safeguards when handling Spectracom equipment.

- Before installing a PCB or other electronic component, discharge static buildup by **touching the metal frame** of the computer/server chassis with one hand, and the protective **antistatic bag** containing the board with the other hand. Open the protective bag only after static buildup has been safely discharged.
- Use a **grounded wrist strap** to prevent static discharge.
- Put components and PCBs **back into their antistatic bags**, while not in use.
- Make sure the unit's chassis, its power supply, and main components are **electrically connected** to one another, so as to allow reliable grounding (if applicable).
- Do not let components or PCBs come into contact with your **clothing**.
- **Handle** PCBs on their edges only; avoid touching electronic components or contacts. If you have to handle a chip, avoid touching its pins.

3.2 GNSS Antenna System Design

For detailed information and recommendations on the design and the installation of GNSS antenna systems, see the Spectracom Antenna System Guide.

3.3 PCIe: Changing the Bracket

The TSync-PCIe board is shipped with a full height card bracket, and a 1/2 height bracket. The latter is pre-installed.

If so required, follow the procedure outlined below to install the full height bracket:

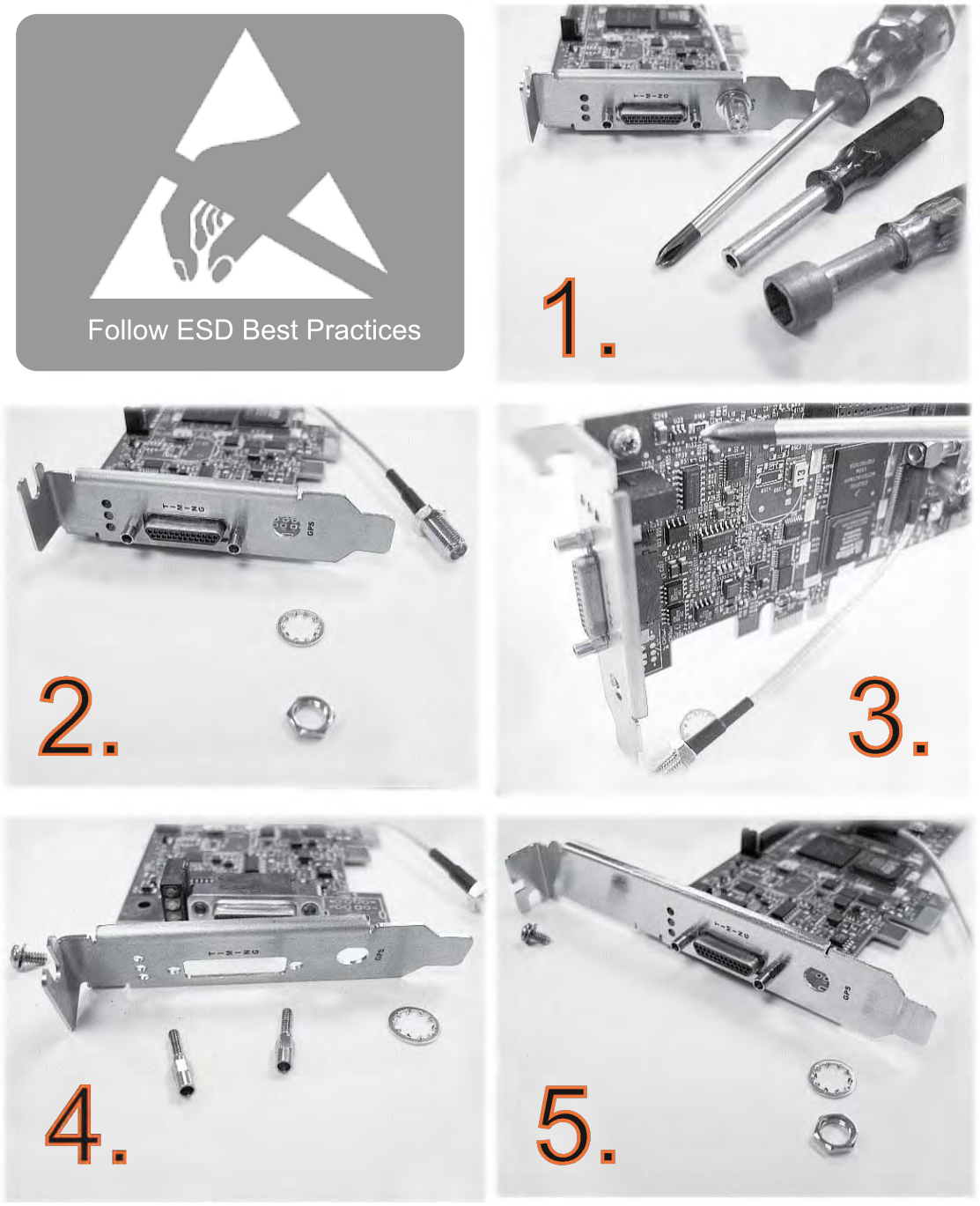

Figure 3-1: Bracket change procedure

Changing the bracket:

1. Tools required for this procedure include a #1 Phillips head screwdriver, a 1/8-inch nut driver or open-end wrench, and a 5/16" driver, wrench, or socket.
2. **Internal GPS receiver boards only**: Using the 5/16-inch driver or wrench, remove the nut and lock washer securing the GNSS RF cable to the board. Slide the cable out of the D-hole in the half-height bracket.
3. Use the Phillips-head screwdriver to remove the Phillips-head screw securing the bracket to the Tsync-PCIe board.
4. Using the 1/8-inch nut driver, remove the two jack screws from the 25-pin connector. The half-height bracket can now be removed from the TSync-PCIe board.
5. Install the full-height bracket. Replace the jack screws on the 25-pin connector.

> **Note:** It may be desirable to install the Phillips-head screw finger-tight, then the jack screws, before completely tightening the Phillips-head screw. Also, be careful to seat the jack screws fully in the holes in the full-height bracket, or the breakout cable will not attach properly to the 25-pin connector when the cable is connected to the board for operation.

6. Reverse steps 1 through 3 in order to complete installation of the full-height bracket. Reconnect the Phillips-head screw to secure the bracket on the board and, for boards with internal GPS receivers, reconnect the SMA RF connector cable (being sure to align it properly in the D-hole).

3.4 Installing the Card

3.4.1 PCIe, cPCI, VPX, PMC: Card Installation

> **Caution:** Always work at an ESD protected workstation, wearing a grounded wrist-strap.

1. Shut the computer down, then turn OFF its power switch, and unplug the line cord. Open the computer chassis.
2. Remove the TSync card from the shipping envelope.
3. Remove the blank computer bracket from the empty slot, and insert the TSync card instead. Attach the top of the TSync bracket with the screw from the metal plate.

   PMC:

Position the card with the standoffs facing the host (carrier) board, and with the I/O-connector oriented toward the front panel. Align the two PCI connectors located at the end of the TSync card opposite the I/O-connector with the mating connectors on the host board, and carefully press the card into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

Attach the card to the host with four 2.5 x 6.5 mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

4. Close the computer, plug in the line cord, and start the computer. Depending on which operating system is used, a message that identifies new hardware may appear. This message may indicate that the hardware is of "unknown type". This is normal. Exit the "Found New Hardware" dialog box.

Note: Once an external GNSS receiver is connected to a cPCI or PCIe card, it will be reset to factory default settings.
If you are replacing an existing legacy board-level product, be aware that your GNSS receiver will no longer operate with legacy board-level products once it has been used with a TSync-cPCI or PCIe board.

3.4.2 PCI-104: Card Installation

Caution: Always work at an ESD protected workstation, wearing a grounded wrist-strap.

1. Turn off power to the PCI-104 system.
2. Select the stand-offs for the desired stack height, and install them (not included).
3. Remove the TSync PCI-104 card from its anti-static bag.
4. Check that the pins of the bus connector are properly positioned.
5. Verify the stacking order. Make sure all of the buses used by the peripheral cards are connected to the CPU-module.
6. Hold the card by its edges and orient it such that the bus connector pins line up with the matching connector on the stack.
7. Carefully and evenly press the card onto the PCI-104 stack.
8. If other cards are to be stacked on top of this unit, install them.
9. Attach any necessary cables.
10. Set the DIP switch in accordance with the card's stack position (see "PCI-104 Configuration (DIP Switch)" on the next page).

11. Re-connect the power cord and apply power to the stack.
12. Boot the system and verify that all of the hardware is working correctly.

The TSync card operates automatically as soon as the host computer system performs the power-on reset. To change the operating parameters or read data, consult the available **Application Programmer's Guide** for this product.

3.4.3 PCI-104 Configuration (DIP Switch)

The max configuration for the PCI bus of PCI-104 modules is FOUR plus the host board. When stacking more than one PCI-104 module to a host board, the modules need to be set to different PCI numbers, using the DIP switch SW1.

Follow the installation procedure outlined under "PCI-104: Card Installation" on the previous page.

Figure 3-2: DIP-switch layout

Table 3-1: SW1 Settings [(*) = default]

Switch 1	Switch 2	Module Slot	INT # selected
OFF (*)	OFF (*)	1	INT A#/CLK 0/IDSEL 0
OFF	ON	2	INT B#/CLK 1/IDSEL 1
ON	OFF	3	INT C#/CLK 2/IDSEL 2
ON	ON	4	INT D#/CLK 3/IDSEL 3

3.5 Status LEDs

TSync Time Code Processor cards include three LEDs that provide visual status information. See table LED Colors below for these indicator codes.

The LEDs operate in certain modes by default, but each LED can be programmed independently to display any mode, including a manual mode. In manual mode, the LEDs are user-

configurable to ON, OFF, or BLINK. For additional information, see the TSync Factory Driver Guide, Section 4.2.8.25 (http://spectracom.com/support/product-manuals-software).

Table 3-2: LED colors

LED Color	Function	Meaning
green	SYNC	Unit is synchronized: A valid external time or 1PPS reference is present, disciplining the oscillator.
yellow	HOLDOVER	Unit is in holdover: No valid external reference is present. The oscillator is not disciplined by an external reference, but continues to provide time/frequency for the duration of the user-set hold-over time (default = 7200 seconds [= 2 hours]).
red	ALARM	The unit does not provide a time or frequency signal.

During the states **power-on**, **self-test**, **wait-for-host**, and **download-from-host**, modes are directly allocated to the LEDs, as listed below.

During **normal operation**, the LEDs can indicate any operational mode, as programmed by the user.

Table 3-3: LED flash patterns

State	Color/FUNCTION		
	green/SYNC	yellow/HOLDOVER	red/ALARM
Power-On	On	Off	Off
Self-Test	On	On	On
Waiting for Host	Blink	Off	Blink
Download from Host	Strobe	Strobe	Strobe
Initialize	Off	Off	Off
Never Synchronized	Off	Off	Off
Synchronized	On	Off	Off
Holdover	On	On	Off
No Longer Synchronized	Off	Off	On
Free Run	Blink	Blink	Off
Fault	Code	Code	Code

The **Fault** state is indicated by the blinking code. It blinks the number of times indicated below, with a 2-second pause between each set.

Table 3-4: Fault codes

No. of Blinks	Meaning
1	FPGA programming error
2	Failure to decompress
3	CRC failure writing to flash
4	Self-test failure
5	Timing system failure

3.6 Upgrades

One of the most powerful features available is the capability to perform field upgrades of the configuration and firmware/FPGA loads for the TSync Time Code Processor cards. New features and capabilities can be added and uploaded to the board without the need to restart the system in which the board is installed. Refer to the Factory Driver Guide for details on upgrading the card using the upgrade tool supplied with the driver.

CHAPTER 4

Theory of Operation

The TSync Time Code Processors architecture comprises **input references**, which are used as sources of 1PPS synchronization and/or time-of-day (TOD, date information, and for disciplining the internal oscillator.

TSync Time Code Processors take the synchronous clock, a 1PPS and time-of-day (TOD) and date to create **output references** that act as time references for other devices.

Other interfaces for time stamping external events, creating precisely timed external signals, debug, upgrade, and access from a host computer are provided.

The following topics are included in this Chapter:

4.1 Theory of Operation

4.1.1 Introduction to GPS and GNSS

The United States Government operates a set of satellites providing positioning, navigation and timing services to users on Earth, in Earth's atmosphere and orbit. This satellite-based Global Positioning System is also known as "GPS Constellation". Other Global Navigation Satellite Systems (GNSS) exist e.g., the Russian GLONASS system, or the European Galileo system.

Each satellite has an internal atomic clock and transmits a signal specifying the time and satellite position. The GPS constellation consists of 24 satellites plus several spares flying in Mid-Earth Orbits (MEO, ~20,000 km), orbiting the earth at a rate of approximately twice per day.

You can determine your position on Earth by listening to four or more satellites, using a GPS receiver. Each satellite transmits a "pulse" at exactly the same time. Depending on your distance from each satellite, you will receive those "pulses" at different times, based on the propagation delay of the radio signal traveling at (near) the speed of light. For the GPS receiver, there are four unknowns in this process – x, y, and z for its position, and the time mark for the start of transmission – hence four satellites minimum are required to obtain a 3D fix by simultaneously solving four equations in order to resolve four unknowns.

The "pulse" is transmitted in the form of a spread spectrum Code Division Multiple Access (CDMA) signal with each satellite using a different Pseudo Random Noise (PRN) code. The CDMA process spreads the "pulse" energy over a long period of time by modulating it into "chips", allowing for a weak signal to be transmitted efficiently by the satellite and reconstructed by the receiver.

The GPS satellites transmit their signals on two different frequencies, L1 (1575 MHz) and L2 (1227 MHz), using two different spread code chip rates: The Coarse/Acquisition (C/A) code is at 1M chips/sec and the Precision (P) code is at 10M/chips/sec. Many commercial receivers in use today only use the L1 C/A signal and can get sufficient accuracy, but a receiver using the P code will get higher accuracy. One that receives both frequencies can further improve accuracy by compensating for variations in propagation delay through the ionosphere.

On top of these timing signals, a low speed data stream (50 bps) is impressed containing the Almanac and Ephemeris data. The Almanac data contains the planned orbital information for each satellite and is valid for many days. The Ephemeris data contains the precise orbital positions of each satellite and is considered valid for about 4 hours. Once the receiver has the position data of the satellites in view, plus the range measurements (sometimes called "pseudo-ranges" because they are only measured estimates, not exact true ranges) to at least four of them, it can then calculate its position on earth.

4.1.2 Characteristics of Other GNSS Systems

All of the global systems operate in a very similar manner to the GPS system, but each has its own unique qualities:

» **GLONASS** – Operates in the L1 band similar to GPS, but uses a Frequency Division Multiple Access (FDMA) signal where each satellite transmits at a slightly different, higher

frequency than GPS. Their orbits are optimized for slightly better accuracy at the northern latitudes, but the system still offers complete worldwide coverage. Originally a relic of the Cold War, the entire constellation was updated and is fully operational with modern equipment since 2011.

- **Galileo** – Uses more modern modulation than GPS, operating in three bands: E1, E5 and E6, and offers an encrypted Public Regulated Service and enhanced Search And Rescue (SAR) service. Only eight satellites are operational today, but birds are being launched in pairs at a faster rate, so a fully operational constellation is expected by 2019.
- **Beidou** (formerly called Compass) - This system is operational regionally over Asia today, but new satellites are being launched to offer full worldwide coverage by 2020 with 37 satellites. The new signal structure is very similar to Galileo and the new GPS signals. In Dec 2012, the Chinese published open system specs so it can be a viable system for worldwide use.
- **QZSS** – A regional navigation satellite system for the East Asia and Oceania region, operated by the Japanese Government. This system is used in combination with data from other GNSS satellites and as such is not operational by itself.

4.1.3 Input References

The input references consist of multiple interfaces to various types of Time References. A Time Reference can take many forms but their fundamental responsibility is they always provide a 1PPS on-time-point, they usually provide a time-of-day and date input and they might provide a control and status protocol to the time source. The input references can also provide other time related data such as Leap Second indication and number of seconds, Julian date, day of year, day of week, week of year, status, sync indication, accuracy indication and other fields unrelated to time.

The TSync Time Code Processor architecture's input reference subsystem is designed to support multiple possible input references, while allowing only a single time reference and 1PPS reference to discipline the local clock subsystem at any given time. The user can choose to use the factory default priority list for input references, or may define a proprietary priority list. This user priority list can be created to combine different time and 1PPS sources (such as GNSS time coupled with the external 1PPS). The user is also provided with the means to enable or disable the selection of a specified input reference allowing them to disregard the list and synchronize to a specific output.

GNSS Receivers as Input References

GNSS receivers are usually the highest precision and accuracy time references a TSync Time Code Processor card can select. GNSS receivers use coaxial GNSS antenna input and typically provides a serial interface and a 1PPS output. The serial interface can be used for bi-directional communication with the GNSS receiver to implement a control and status protocol which conveys time and position information.

IRIG Inputs

Inter-range instrumentation group time codes, more commonly referred to as "IRIG" time codes, were created by the Tele-Communications Working Group of the Inter-Range Instrumentation Group, which is a standard body formed by Range Commanders Council. This standard was used by US Government military test ranges, NASA, and other research organizations to distribute telemetry information, including time and frequency. The current standard version is IRIG Standard 200-4. The TSync Time Code Processor architecture uses IRIG formats as both input and output references. IRIG formats can be amplitude modulated, or they can be digital signals at various carrier and clock rates.

The TSync Time Code Processor architecture supports IRIG inputs with Formats A, B, and G. It supports inputs and outputs using modulation frequency values of pulse width code, also known as DCLS (0), and sine wave amplitude modulated coding. Additionally, the card supports inputs with frequency/resolution values of no carrier/index count interval, 1kHz/1ms, 10 kHz/0.1 ms, and 100 kHz/10 ms, as well as IRIG input coded expressions of the fields BCDTOY, CF, SBS, and BCDYEAR.

TSync Time Code Processor cards support IRIG inputs of the following coded expressions combinations for BCDTOY, CF, SBS, and BCDYEAR fields:

- 0 – BCDTOY, CF, SBS
- 1 – BCDTOY, CF
- 2 – BCDTOY
- 3 – BCDTOY, SBS
- 4 – BCDTOY, BCDYEAR, CF, SBS
- 5 – BCDTOY, BCDYEAR, CF

TSync Time Code Processor cards support synchronization with the following analog and DCLS IRIG input formats:

Table 4-1: IRIG Input Reference Formats

A – DCLS	A – AM	B – DCLS	B – AM	G – DCLS	G – AM
A – DCLS	A – AM	B – DCLS	B – AM	G – DCLS	G – AM
A000	A130	B000	B120	NA	NA
A001	A131	B001	B121	G001	G141
A002	A132	B002	B122	G002	G142
A003	A133	B003	B123	NA	NA
A004	A134	B004	B124	NA	NA
NA	NA	NA	NA	G005	G145

TSync Time Code Processor cards support the IRIG B variant NASA36 as an input format, as well as the IEEE C37.118-2005 (which is an IRIG B format with extensions as an input format). The IEEE C37.118-2005 specification supersedes IEEE 1344-1996. The TSync Time Code Processor is backward compatible to IEEE 1344-1996 by compliance with IEEE C37.118-2005.

The card can automatically detect IRIG formats A, B, G, and NASA36. However, IRIG format IEEE1344, coded expression, and control field information cannot be auto-detected. These must be specified by the user if these inputs are to be used.

Note: Always configure IRIG parameters in the following order: format, coded expressions, control field definitions.

In operation, the TSync Time Code Processor card receives IRIG input data and any time code messages transmitted, performs signal conditioning on the data, and decodes the data per its manually set parameters and automatically detected functions. In turn, the card provides a serial time code data message and a 1PPS reference. It also returns the IRIG input message's raw serial time code data in Spectracom's data format. (This is useful in debugging serial time code source and hardware implementations.)

TSync Time Code Processor cards also accept as input any non-standard IRIG format generated by Spectracom Netclock units, including the non-standard BCDYEAR found in the Control field. This is intended to support the Spectracom 91xx and 92xx IRIG formats, which use the BCDYEAR in the Control field.

External 1PPS Reference

The card's external 1PPS reference provides the on-time-point for the current second. This reference is used by the TSync Time Code Processor as the primary source of frequency synchronization (while another input reference is required to serve as the source of time and date information). The external 1PPS reference can be set to use either the rising or falling edge.

4.1.3.1 Built-in References

The TSync Time Code Processor card provides built-in references that support specialized user applications.

Host Reference

The TSync Time Code Processor can be set to use the host as the source of date and time information, while another input reference is required to serve as the source of frequency input. This allows the host to provide time to the card while providing a means to determine and indicate whether that time is valid for synchronization. Using the host as a reference means it could conceivably be used to receive date and time information from a source not available to the card, providing that information to the card for synchronization to it (while using a separate frequency input).

Self Reference

The TSync Time Code Processor provides a built-in reference that allows the card to operate without a separate input reference. The date and time or frequency information from this self reference is always considered valid. This allows a user to operate the card as if it were synchronizing to an input reference, without a valid external reference input. The self reference priority table entry defaults to “disabled.”

4.1.4 Input Reference Monitor

The input reference monitor subsystem maintains the reference priority table and determines which input reference(s) are selected to synchronize the clock subsystem.

Three tables are maintained by the system:

- A default table, which provides the default reference pairings in timing accuracy priority
- A working table, which is the table used for selecting reference inputs
- A user table, which can be stored persistently and, if present, will be loaded into the working table at startup.

Table 4-2: Example default table

Enable	Priority	Time Ref	1PPS Ref
en	1	gps0	gps0
en	2	ird0	ird0
en	3	ira0	ira0
en	4	hst0	epp0
en	5	hst0	self
dis	6	self	self
dis	0		
dis	0		

Legend: gps = GPS Reference, ird = IRIG DCLS Reference, ira = IRIG AM Reference, epp = External 1PPS Reference, hst0 = Host Reference, self = Self Reference

Entries can be added to and deleted from the working table. In addition, individual entries can be enabled or disabled. Their priorities can be changed at any time. Any changes to the table will cause the reference monitor to reevaluate the best reference to use for synchronization. The working table can be saved to the user table and persisted, or it can be reset to the default table or an already existing user table at any time.

At any given time, the highest priority enabled entry in the table that has both a valid time and a valid 1PPS reference will be used as the best reference for synchronization. The power of the reference monitor is in its ability to generate any combination of time and 1PPS references in any priority. For example, if a user has a high precision 1PPS source, this can serve as the provided external 1PPS reference and can be paired with a GNSS time reference.

The reference tables, the currently selected best reference, and the current validity states of all input references can be requested from the card.

4.1.5 Clock Subsystem

The clock subsystem is the heart of the TSync Time Code Processor timing architecture. Time is maintained in the card's hardware and incremented in 5nsec units, while sub-second

information is tracked. Time, from seconds through years, is incremented based on the internal 1PPS derived from the selected input reference.

By default, system time is maintained in UTC, but this can be set to TAI, GPS, or a local timescale (with DST rules). Offsets between timescales are maintained on the card to facilitate conversions between the timescales. The offsets can be set by the user or, depending on the references available, may be automatically determined. Users who wish to use a specific timescale must provide the timescale offset from an input reference or by setting it manually.

The clock subsystem can handle several types of time discontinuities, including leap years, leap seconds, DST transitions, and a user-settable discontinuity. Leap years are automatically detected and handled by the system. Leap seconds, if set from the user or received from an input reference, are also handled accordingly. The system can manage DST transitions set by the user when running in a local timescale.

4.1.6 Output References

The output subsystem provides time code and frequency references derived from the input reference. The outputs provided include a single IRIG AM and DCLS output pair, a 10-MHz sine wave output, and a 1PPS output.

The output subsystem supports setting output offset(s) for each output except the 10-MHz sine wave output, which can be used to compensate for output cable length delays or downstream clock accuracy errors. Each output offset can range from -500 msec to +500 msec in 5 or 20-nsec steps (depending on the type of output).

IRIG Output

The TSync Time Code Processor card provides one IRIG AM and DCLS pair output. The IRIG output is a rolling count of the initial value of the system time until synchronized. The card drives the IRIG AM output from an associated IRIG DCLS output and outputs the exact same format (except for the AM modulation).

The TSync Time Code Processor card supports IRIG outputs with Formats A, B, E and G. It also supports IRIG outputs using modulation frequency values of pulse width code, also known as DCLS, and sine wave amplitude modulated coding. It further supports IRIG outputs with frequency/resolution values of no carrier/index count interval, 100 Hz/10 ms, 1kHz/1ms, 10 kHz/0.1 ms, and 100 kHz/10 ms. Coded expressions for the fields BCDTOY, CF, SBS, and BCDYEAR. Are supported, as is IRIG output for the following coded expressions combinations for BCDTOY, CF, SBS, and BCDYEAR fields:

- 0 – BCDTOY, CF, SBS
- 1 – BCDTOY, CF
- 2 – BCDTOY
- 3 – BCDTOY, SBS
- 4 – BCDTOY, BCDYEAR, CF, SBS
- 5 – BCDTOY, BCDYEAR, CF

TSync Time Code Processor cards allow the user to select the following Time Code Formats for IRIG output:

Table 4-3: IRIG Output Reference Formats

A – DCLS	A – AM	B – DCLS	B – AM	E – DCLS	E – AM	G – DCLS	G – AM
A000	A130	B000	B120	E000	E110	NA	NA
A001	A131	B001	B121	E001	E111	G001	G141
A002	A132	B002	B122	E002	E112	G002	G142
A003	A133	B003	B123	E003	E120	NA	NA
A004	A134	B004	B124	E004	E122	NA	NA
NA	NA	NA	NA	E005	E125	NA	G145

TSync Time Code Processors allow the user to select the IRIG B variant NASA36 as an IRIG output. It also supports user-selection of IEEE C37.118-2005 as an IRIG output. This is an IRIG B format with extensions. The card is compliant with IEEE 1344-1996 as IEEE C37.118-2005 supersedes this specification.

The card generates the non-standard IRIG formats that are generated by the Spectracom Netclock, including the non-standard BCDYEAR. This provides for compatibility with existing Spectracom NetClock products.

Note: Configuration of IRIG parameters should always be in the following order: format, coded expressions, control field definitions.

TSync Time Code Processor cards support adjustment of the IRIG output amplitude using a scale ranging from 0 to 255, with 128 being the middle and default value. The adjustment range approximates a linear function.

The IRIG outputs provide an offset that can be applied to adjust its relationship with the internal system 1PPS, from -500 msec to +500 msec in 5-nsec increments

The IRIG outputs provide signature control, which enables and disables outputs under the following conditions:

- Signature control off — outputs always on.
- Signature control enables output when in sync to input reference only
- Signature control enables output when in sync to input reference or in holdover.

10 MHz Sine Wave Output

TSync Time Code Processor cards generate a 10 MHz sine wave output from the disciplined on-board oscillator. The 10 MHz sine wave output provides signature control similar to the IRIG outputs.

1PPS Output

TSync Time Code Processor cards generate a digital 1PPS output from the internal 1PPS of the system. Several parameters of the 1PPS can be controlled. The active edge can be set to either rising or falling edge, the pulse width can be adjusted, and an offset can be applied to adjust its relationship to the internal system, 1PPS from -500 msec to +500 msec in 5nsec increments. The 1PPS output provides signature control similar to the IRIG outputs.

4.1.7 General Purpose Input/Output

TSync Time Code Processor cards have four general purpose input (GPIO) pins and four general purpose output (GPIO) pins. The General I/O subsystem provides a mechanism to generate or time stamp external events, to match times and generate a signal, to create Heartbeat pulses, or to create square wave clock signals synchronous to the internal timing system clock and to the 1PPS signal from the input reference.

4.1.7.1 Programmable Inputs

The General I/O input pins support user selection for detection of rising edge or falling edge input events. These inputs, when triggered, are used to time-tag the input edge-detected events. They support a time between input events of 50 nsec and an overall rate of more than 10,000 time stamps per second. Time stamps are maintained in a FIFO manner on the board that can store up to 512 unique time stamps among all input pins.

4.1.7.2 Programmable Outputs

The user may select the operational mode of the General I/O outputs pins, setting them to generic output pins, square wave generation, and match time events.

The General I/O outputs, when configured as generic output pins, can be controlled and changed at the user's discretion.

The General I/O output can be programmed as a square wave synchronized to the 1PPS. When used to output a square wave, the General I/O has a programmable period range of 100 nsec to 1sec (10 MHz to 1Hz) in 5nsec steps and a programmable pulse width of 10 nsec to 999,999,990 nsec in 5nsec steps (polarity is programmable).

The General I/O is configurable as a Match Time Event pin, which will activate at a preset time and become inactive at another preset time. The Match Time Event provides two user settable times to make the General I/O pin active and inactive. The Match Time Event configured General I/O pin has a programmable edge, allowing the selection of Low to High or High to Low.s

The General I/O output signals timing are accurate relative to the Input reference's 1PPS signal to within ±50 nsec. The General I/O output has a programmable offset, which ranges from –500 msec to +500 msec in 5nsec steps.

4.1.8 Interrupts

The host bus has one interrupt line available from the TSync Time Code Processor. All interrupt sources destined for the host bus are multiplexed on the single interrupt line. All interrupts are masked on startup, but can be unmasked using the host bus interrupt mask register. Whether an interrupt is masked or not, the current state of the interrupt is available by reading the Host Bus Interrupt Status register. All interrupt sources are latched based on an edge transition. All interrupts are cleared in the host bus interrupt status register.

4.1.8.1 Interrupt Descriptions

1PPS Received

This interrupt is driven on the incident edge of the PPS.

Timing System Service Request

This interrupt is used by the micro to request attention from the local bus.

Local/µC Bus FIFO Empty

This interrupt is driven when the FIFO from the local bus to the microcontroller bus becomes empty. It is based on the rising edge of the FIFO's empty flag.

Local/µC Bus FIFO Overflow

This interrupt is driven when the FIFO from the local bus to the microcontroller bus is overflowed. It is based on the rising edge of the FIFO's overflow flag.

µC/local bus FIFO Data Available

This interrupt is driven when the FIFO from the microcontroller bus to the local bus is no longer empty. It is based on the falling edge of the FIFO's empty flag.

µC/local bus FIFO Overflow

This interrupt is driven when the FIFO from the microcontroller bus to the local bus is overflowed. It is based on the rising edge of the FIFO's overflow flag.

GPIO Input x Event

This interrupt is driven when the active edge of the GPIO input signal is received.

GPIO Output x Event

The interrupt is driven when an event occurs in the GPIO output. An event depends on the mode of operation of the GPIO output. In Direct mode, an event is triggered when the output Value in the GPIO output control / status register is changed and creates the active edge selected by the GPIO direct mode output interrupt active edge bit in that same register. This can be used to generate a "software" interrupt by setting the GPIO output appropriately. In match time mode, an interrupt is generated whenever the GPIO output high match time or GPIO output low match time registers are enabled and subsequently matched against the current system time. In square

wave mode, an interrupt is generated whenever the GPIO output generates the active edge as selected by the GPIO output square wave active edge bit in the GPIO output control / status register. This can be used to generate a periodic interrupt at the rate of the square wave.

Time Stamp Data Available

This interrupt is driven when the time stamp FIFO goes non-empty. Time stamp data is available in the time stamp FIFO when this interrupt occurs.

4.2 Configuration and Operation

4.2.1 Configuring the TSync Product

TSync cards can be adapted to your application by utilizing the following functionality:

4.2.1.1 Interrupts

The card generates interrupts that can then be queried. For example, a 1PPS interrupt can be generated that can be utilized via a WAITFOR blocking call. Available interrupts are listed under "Interrupts" on the previous page.

4.2.1.2 Match Time

Using one or several of the four General Purpose Outputs (GPO's), a Match Time signal can be sent out, in order to trigger an event at a preset time, e.g. during a simulation.

4.2.1.3 Time Stamping

Using one or several of the four General Purpose Inputs (GPI's), an event can be sent to the TSync card that will then be time stamped by the card. An application example would be a camera shutter signal that can be used to assign a time stamp to an image captured.

4.2.2 Synchronizing a Linux Machine Using NTP

TSync boards can also be used to provide very accurate time stamps via the PC's bus system to either NTPv4 (freeware) or Spectracom TimeKeeper software running on the TSync host computer. In order to be able to synchronize Linux using NTP, the 3rd party NTP module (if not already included in the Linux kernel on your machine) must be downloaded, as described below in detail. This module includes the Reference Clock Driver that gets applied as a patch to the Linux driver.

Important Note:

1. The NTP patch for syncing NTP via an installed TSync timing board is only available in the Linux drivers for Spectracom bus-level timing boards. It is not provided in the Solaris driver. Solaris can only be synced via NTP time stamps from a networked NTP time server or via ASCII time stamps from the Serial output port of a Spectracom time reference.

Note: NTPv4.2.8 and above now include the TSync reference clock driver, i.e. it is no longer necessary to patch NTP using the NTP patch in the Spectracom Linux driver.

Windows, Linux and Solaris drivers for TSync boards are available from Spectracom. The Linux driver files contain README files. The README file contains the instructions to configure the timing card as a reference time source for NTP.

In summary of the instructions in the README file, with NTP software already installed on the PC, the driver contains a patch that is installed into the NTP software. Once the NTP patch has been installed into the NTP software, the NTP software is then recompiled and is then run from the newly compiled location. With the patch applied, NTP can then obtain time from the Spectracom timing board.

The Linux machine with NTP software compiled and with a TSync board installed can be made into an NTP Server that can provide time to synchronize the rest of the network. Refer to the NTP website of http://www.ntp.org/ to obtain both the NTP software and more information on how to build and configure NTP to be a network time server. In this scenario, the computer is synced to the timing board and the network clients are synced to the PC.

Please note that the instructions for the NTP patch were written for a specific version NTP version of NTP (please refer to the README file for the most current, specified version of NTP to use). If another version of NTP is installed on the computer, other changes not listed in the README file may be required to make the timing card work with that particular version of NTP.

Specific Notes about the Linux driver NTP README file:

1. When using an IRIG input to synchronize the timing card, the current year needs to be either automatically calculated by the timing card based on the IRIG input, or it must be manually entered by you.
2. After installing the patch and then recompiling NTP, run NTP from the newly compiled location.
3. Use the "-g" switch to start NTP.
4. Make sure the PC is within ±4hours of the time reported by the TSync board. NTP will not correct a time offset of a PC that is greater than 4 hours.
5. Based on customer feedback, the `NTP.conf` file may need to be edited. The "keys" made need to be rem'd out in order for NTP to use the timing board as its reference.

Note regarding synchronization of the TSync board: When using a TSync board to sync NTP, the TSync board itself must be synced to IRIG or GPS. However, it can also be manually synced

using the hst1/epp0 input references. The TSync board can declare sync with the self/epp0 input references, but NTP will not sync to the board with these input references being used to sync the timing board. The minimum requirement for NTP synchronization is hst1/epp0.

4.2.3 Synchronizing a Windows Machine Using NTP

In order to synchronize a Windows computer via NTP, use the **clock daemon** and the **clock utility**, as described in the Factory Driver Guide. See also the Tech Note Synchronizing Windows Computers.

4.2.4 Resetting a TSync Card

In order to reset all TSync card settings, the host computer must be **powered down**, since during a reboot of the host computer, the TSync card will NOT lose all of its settings.

The card can also be reset using the **Reset API** call. In both cases, no volatile settings are stored with the exception of the Reference Priority Table, i.e. the start-up script needs to be run again in order to re-initialize the system and reset all settings from their factory default values to their designated values.

Please note that – contrary to GPS – IRIG references do not automatically set the Year during startup, i.e. the TSync defaults to its factory default setting, the year 2000 (Note that TSync cards do not have a Real Time Clock, hence the factory default Year will be applied). In your startup script, you have to run a call pointing to the specific location in the IRIG Control Function section or BCD string where the Year information is located.

4.2.4.1 About Volatility

For information on memory volatility, see the Tech Note Certificate of Volatility.

4.2.5 Powering UP/DOWN a GNSS Receiver

When power is first applied to a GNSS receiver, it begins looking for satellites. It does this by searching for each satellite, individually, listening for every satellite's distinct spread-spectrum hopping sequence. This process can take several minutes, as the receiver iteratively locates satellites, refines its position, and determines for which satellites to search.

When the power is switched off, a GNSS receiver retains the last known position. This typically results in faster satellite acquisition the next time it is switched on, because the receiver will use the previously mentioned Almanac data to locate the satellites. If, however, the antenna has been moved more than a few miles, or too many days have passed since the power had been turned off, acquisition time will be longer.

4.2.6 System Status

TSync Time Code Processor cards maintain status information: They log error and informational messages while operational. Accessible system status information includes:

- synchronization status
- holdover status
- freerun status
- total system uptime.

In addition, alarm conditions and time stamps for the alarms are available for conditions including synchronization, holdover, frequency errors, PPS specification errors, reference changes, and system errors.

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CHAPTER 5

Options and Accessories

This Chapter describes the breakout cables, and the timing interface adapter cables.

5.1 Accessories & Options

In the standard configuration, all TSync Time Code Processors are equipped with a TCXO oscillator. As an option, TSync Time Code Processors can be ordered with an OCXO oscillator, or a Rugged OCXO oscillator.

PCIe, PMC: Timing Interface Adapter Cable

PCIe and PMC cards are shipped with a 15 cm(6")-adapter cable that is is used to connect the micro 25-pin timing interface connector on the card to the breakout cable:

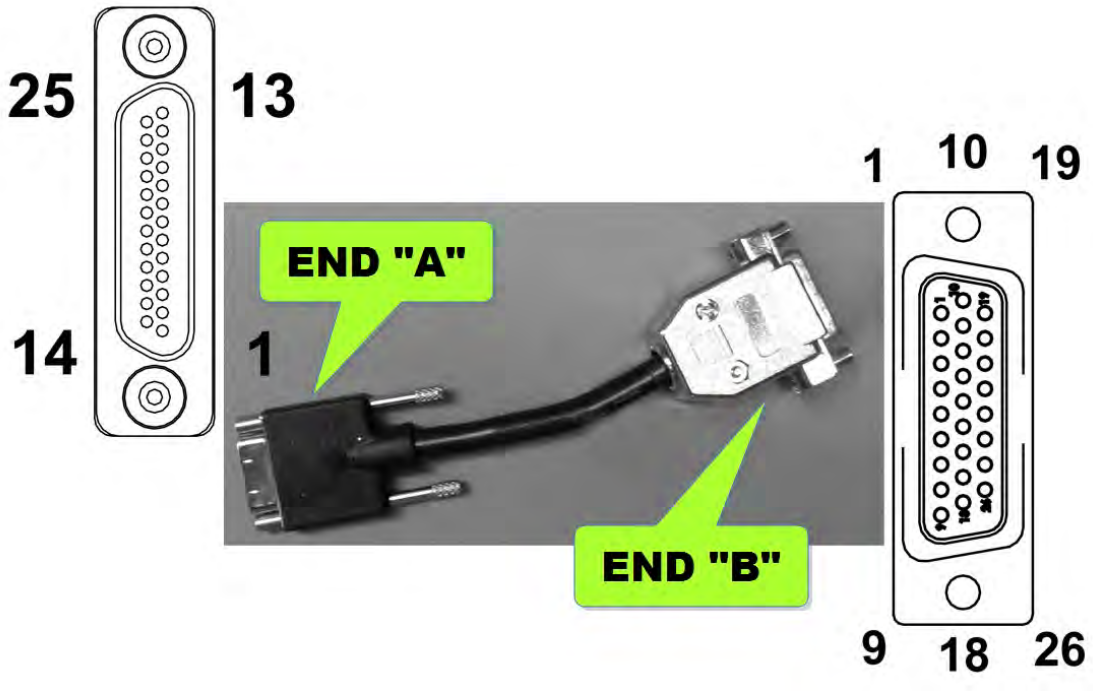

Figure 5-1: Adapter cable

Table 5-1: Adapter pinout, timing connector

END "A"	END "B"
PIN-1	PIN-1
PIN-2	PIN-2
PIN-3	PIN-3
PIN-4	PIN-4
PIN-5	PIN-5

END "A"	END "B"
PIN-6	PIN-6
PIN-7	PIN-7
PIN-8	PIN-8
PIN-9	PIN-9
PIN-10	PIN-10
PIN-11	PIN-11
PIN-12	PIN-12
PIN-13	PIN-13
PIN-14	PIN-14
PIN-15	PIN-15
PIN-16	PIN-16
PIN-17	PIN-17
PIN-18	PIN-18
PIN-19	PIN-19
PIN-20	PIN-20
PIN-21	PIN-21
PIN-22	PIN-22
PIN-23	PIN-23
PIN-24	PIN-24
PIN-25	PIN-25
NO CONNECT	PIN-26 SHIELD

Basic Breakout Cable

The basic breakout cable breaks out a subset of features from the 26-pin timing connector to separate BNC and DB-9 connectors for use. The basic breakout cable supports the following features: External 1PPS Input, IRIG AM Input, IRIG DCLS Input, IRIG AM Output, (1) GP Input, (2) GP Outputs.

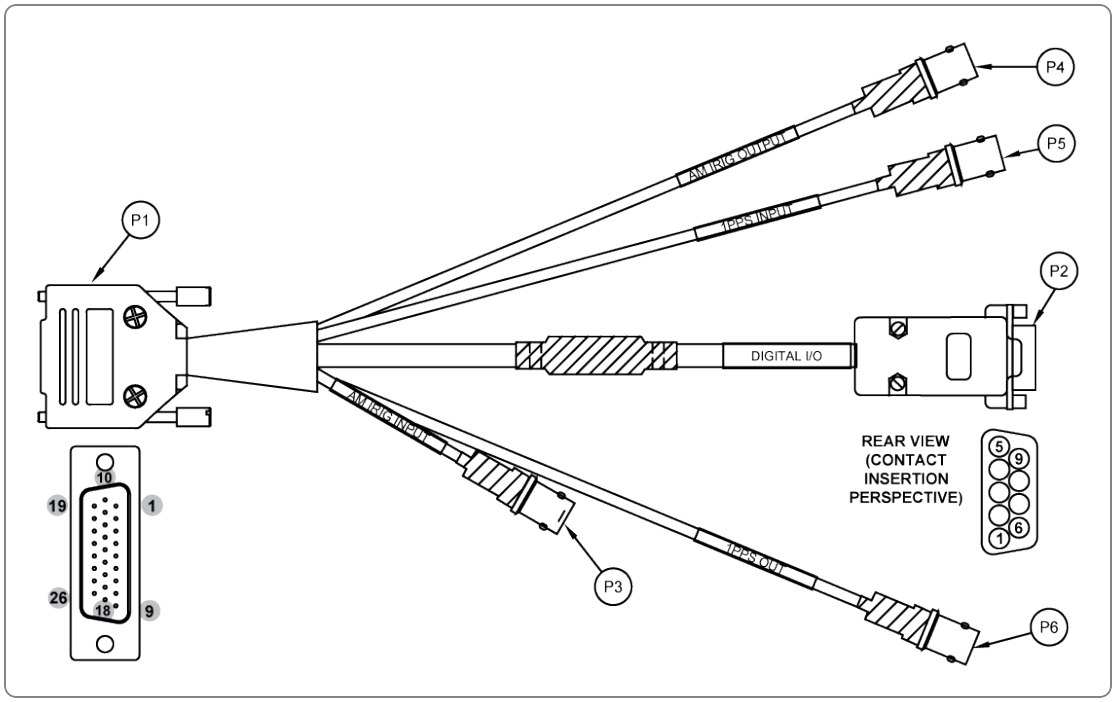

Figure 5-2: Breakout cable, basic version

Table 5-2: Pinout, basic breakout cable (unspecified pins in the table are not connected)

Pin	Signal	Pin	Signal
P1—Timing Connector			
3	GPIO Output 0	11	IRIG AM Input -
5	Ground	16	GPIO Output 1
6	GPIO Input 0	18	Ground
7	External 1PPS Input	21	Ground
8	Ground	24	IRIG DCLS Input -
9	IRIG AM Output	25	IRIG DCLS Input +
10	IRIG AM Input +		
P2—Digital I/O (DB-9 Female)			
1	Ground	6	GPIO Output 0
2	GPIO Input 0	7	Ground
3	Ground	8	GPIO Output 1

Pin	Signal	Pin	Signal
4	IRIG DCLS Input +	9	Ground
5	IRIG DCLS Input -	BS	Ground
P3—IRIG AM Input (BNC Female)			
1	IRIG AM Input +	BS	IRIG AM Input -
P4—IRIG AM Output (BNC Female)			
1	IRIG AM Output	BS	Ground
P5—1PPS Input (BNC Female)			
1	External 1PPS Input	BS	Ground
P6—1PPS Output (BNC Female)			
1	1PPS Output	BS	Ground

Premium Breakout Cable

The premium breakout cable breaks out all features from the timing connector to separate BNC and DB-9 connectors for use. See table below for details.

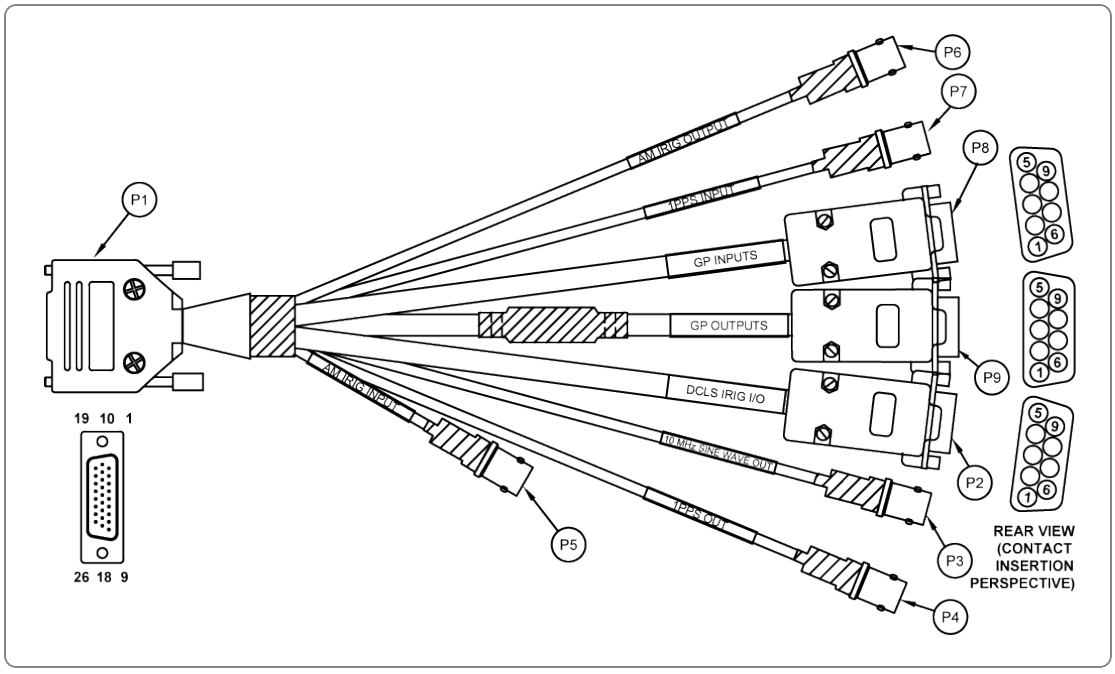

Figure 5-3: Breakout cable, premium version

Table 5-3: Pinout, premium breakout cable (unspecified pins are not connected in the cable)

Pin	Signal	Pin	Signal
P1—Timing Connector			
1	GPIO Output 2	14	GPIO Output 3
2	Ground	15	Ground
3	GPIO Output 0	16	GPIO Output 1
4	GPIO Input 2	17	GPIO Input 3
5	Ground	18	Ground
6	GPIO Input 0	19	GPIO Input 1
7	External 1PPS Input	20	1PPS Output
8	Ground	21	Ground
9	IRIG AM Output	22	10MHz Output
10	IRIG AM Input +	23	Ground
11	IRIG AM Input -	24	IRIG DCLS Input -
12	IRIG DCLS Output -	25	IRIG DCLS Input +
13	IRIG DCLS Output +	26	Shield
IRIG DCLS I/O (DB-9 Female)			
2	Ground	6	IRIG DCLS Output +
3	Ground	7	IRIG DCLS Output -
4	IRIG DCLS Input +	BS	Ground
5	IRIG DCLS Input -		
P3—10MHz Output (BNC Female)			
1	10MHz Output	BS	Ground
P4—1PPS Output (BNC Female)			
1	1PPS Output	BS	Ground
P5—IRIG AM Input (BNC Female)			
1	IRIG AM Input +	BS	IRIG AM Input -
P6—IRIG AM Output (BNC Female)			
1	IRIG AM Output	BS	Ground

Pin	Signal	Pin	Signal
P7—1PPS Input (BNC Female)			
1	External 1PPS Input	BS	Ground
P8—GP Input (DB-9 Female)			
1	GPIO Input 0	7	Ground
2	GPIO Input 1	8	Ground
3	GPIO Input 2	9	Ground
4	GPIO Input 3	BS	Ground
6	Ground		
P9—GP Output (DB-9 Female)			
1	GPIO Output 0	7	Ground
2	GPIO Output 1	8	Ground
3	GPIO Output 2	9	Ground
4	GPIO Output 3		
6	Ground	BS	Ground

GNSS Cables

Contact Spectracom for more information on GNSS cable length options.

PCIe, cPCI

Figure 5-4: PCIe DIN-DB15 adapter cable

If your TSync Time Code Processor board is configured to be operated with a smart antenna, it will have shipped with a GPS/GNSS data adapter cable. For more information see "External Antenna Connector: Pinout" on page 18.

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CHAPTER 6

Driver Support

Using the Spectracom TSync factory driver package, you may configure your card using the API library, so as to support your unique applications.

Factory Driver Guide

The TSync Factory Driver supports Linux, Windows and Solaris. The Factory Driver Guide includes instructions on:

- how to **install/uninstall** the driver
- **upgrading** Firmware
- the **Control Utility**
- the **Clock Daemon**
- **API calls**, their syntax and values.

Application Programmer's Guide

The Application Programmer's Guide documents the Host Interface Protocol (HIP), and the Public Message API and a listing of its transactions, among other things.

Further reading:

- For a listing of interrupts, see "Interrupts" on page 39.
- For the TSync Factory Driver Guide, and the Application Programmer's Guide, see http://spectracom.com/support/product-manuals-software/.
- For a listing of all supported API calls, see Table 4.1 in Section 4.2.7 of the Factory Driver Guide.

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APPENDIX

Appendix

The following topics are included in this Chapter:

7.1 YOUR SAFETY

This topic contains information that is relevant not only for your personal safety, but can also help prevent potential damage when working with the equipment.

Figure 7-1: Do not ignore the Safety Instructions!

7.1.1 Spectracom Safety Symbols

The following symbols are used in Spectracom technical documentation, or on Spectracom products:

Table 7-1: Spectracom safety symbols

Symbol	Signal word	Definition
	DANGER!	Potentially dangerous situation which may lead to personal injury or death! Follow the instructions closely.
	CAUTION!	Potential equipment damage or destruction! Follow the instructions closely.
	NOTE	Tips and other useful or important information.
	ESD	Risk of ElectroStatic Discharge! Avoid potential equipment damage by following ESD Best Practices.
	CHASSIS GROUND	This symbol is used for identifying the functional ground of an I/O signal. It is always connected to the instrument chassis.

Symbol	Signal word	Definition
	Analog Ground	Shows where the protective ground terminal is connected inside the instrument. Never remove or loosen this screw!
	Recycle	Recycle the mentioned components at their end of life. Follow local laws.

7.1.2 About Safety

This product has been designed and built in accordance with state-of-the-art standards and the recognized safety rules. Nevertheless, its use may constitute a risk to the operator or installation/maintenance personnel, if used under conditions that must be deemed unsafe, or for purposes other than the product's designated use, which is described in the introductory technical chapters of this guide.

7.1.3 Your Responsibilities

- The equipment must only be used in technically perfect condition. Check components for damage prior to installation. Also check for loose or scorched cables on other nearby equipment.
- Make sure you possess the professional skills, and have received the training necessary for the type of work you are about to perform (for example *Best Practices in ESD prevention*.)
- Do not modify the equipment, and use only spare parts authorized by Spectracom.
- Always follow the instructions set out in this guide.
- Observe generally applicable legal and other local mandatory regulations.

7.1.4 Other Safety Tips

Keep these instructions at hand, near the place of use.

Keep your workplace tidy.

Apply technical common sense: If you suspect that it is unsafe to use the product, do the following:

- Disconnect the supply voltage from the (main) unit, e.g. by unplugging the line cord.
- Clearly mark the equipment to prevent its further operation.

7.2 Technical Support

To request technical support, please go to the "Support" page of the Spectracom Corporate website, where you can not only submit a support request, but also find additional technical documentation.

Phone support is available during regular office hours under the telephone numbers listed below.

To speed up the diagnosis of your TSync Time Code Processor unit, please send us:

- your current **product configuration**, and
- the **events log**.

Thank you for your cooperation.

7.2.1 Regional Contact

Spectracom operates globally and has offices in several locations around the world. Our main offices are listed below:

Table 7-2: Spectracom contact information

Country	Location	Phone
China	Beijing	+86 10 8231 9601
France	Les Ulis, Cedex	+33 (0)1 64 53 39 80
USA	Rochester, NY	+1 585 321 5800

Additional regional contact information can be found on the Contact page of the Spectracom Corporate website.

7.3 Return Shipments

Please **contact** Spectracom **Technical Support** before returning any equipment to Spectracom. Technical Support must provide you with a **Return Material Authorization** Number (RMA#) prior to shipment.

When contacting Technical Support, please be prepared to provide your equipment **serial number**(s) and a description of the **failure symptoms** or issues you would like resolved.

Freight to Spectracom is to be prepaid by the customer.

Note: Should there be a need to return equipment to Spectracom, it ought to be shipped in its original packing material. Save all packaging material for this purpose.

List of Tables

List of Images

Document Revision History

Previous editions of this manual:

Product	Part No.	Revision	ECO number	Date
PCIe	1191-5000-0050	H	45	20-May-2014
cPCI	1219-5000-0050	4	422	5-May-2014
PCI-104	1220-5000-0050	A	45	20-May-2014
PMC	1221-5000-0050	B	45	20-May-2014
VPX	1226-5000-0050	1	n/a	2-May-2015

Current edition of this manual (Part no.: 1226-5000-0050)

Revision	ECO	Description	Date
1	n/a	User Manual Addendum, covering VPX board related information only.	2-May-2015
2	589	Consolidated previous editions of TSync manuals, and added information for the VPX board.	14-March-2016

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